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Design of a PTC-Inspired Segmented ADC for High-Speed Column-Parallel CMOS Image Sensor

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Abstract
This paper presents a successive approximation ADC (SAR) architecture that takes advantage of the signal-dependent photon shot-noise characteristic of an image sensor. The multi-segmented successive approximation ADC (MS-SAR) applies the sub-ranging technique, where each segment's conversion step size is scaled according to the photon transfer curve (PTC) of a given pixel. The MS-SAR selects the appropriate segment with a binary search and then resolves the remaining bits with the SAR register. The ADC is designed to be highly scalable and is targeted for a family of image sensors requiring high-resolution A/D converters. A first prototype high-speed column-parallel image sensor using the MS-SAR architecture was fabricated in a 0.18 um 5V/1.8V CMOS process. Measurement results from this demonstrate that the ADC is capable of resolving 16 bits at the lowest segment with a conversion time of 2.475 us.

I. Introduction

The demand for high-resolution, high-frame-rate, high dynamic range, and low-noise CMOS image sensors continues to push the technology of our pixel readout circuitry. We see an increasing requirement for higher resolution ADCs, with the next generation at 16 bits. The need for low-noise, high-bit resolution is especially important in low light levels, where the readout noise may not be dominated by photon shot noise. Inspired by the well-known PTC response of an image sensor, as well as by earlier work on single-slope ADCs, we have designed an ADC whose resolution can be scaled with the input signal level. This concept was demonstrated in [1][2], where the authors used an accelerated-ramp, single-slope ADC, and was also applied in [3] with a multi-ramp, multi-slope approach. All designs took advantage of the PTC characteristic to reduce the conversion rate of the single-slope ADC.

In this paper we present a segmented successive approximation ADC architecture that takes advantage of the PTC characteristic and scales its bit resolution with the input signal. The main motivation here, along with a faster conversion rate, is to overcome design problems and increase the resolution of the SAR ADC for a column-parallel CMOS image sensor.

II. ADC Architecture

Successive approximation ADC architecture is most suitable for high-performance CMOS image sensors when both fast conversion speeds and high-bit resolution are required. A number of papers have shown steady increases in column-parallel SAR ADC resolutions. The most recent paper reported a 14-bit ADC using three different reference voltages [4]. As we attempt to further scale up the ADC resolution, new design challenges emerge:

> **ADC Area**: The area taken up by the DAC increases by 2^N number of bits. Using multiple numbers of reference voltages, we can limit the overall capacitor size, but this then poses the challenge of generating accurate voltage references to achieve good ADC DNL.

Capacitor Matching: A second challenge is to overcome the capacitor ratio-matching requirement: for each N-bit converted, the capacitor ratio must match to the given resolution. This is especially difficult for narrow-pitch layouts and small pixel dimensions.

Reference Voltage Settling: As pixel array size increases, so does the challenge of settling the voltage references. This challenge grows with increased SAR capacitor sizes and higher bit counts.

Our proposed solution to these design challenges is a multi-segmented SAR where each segment's ADC resolution is adjustable with varying voltage reference levels. Figure 1 shows a simplified block diagram of the MS-SAR ADC architecture. The ADC consists of the selection logic for the multiple sub-ranging segments, the residual fine successive approximation registers, and a high-gain comparator. In our design we chose to have a total of 8 segments that resolve the coarse 3 MSB of the ADC. The conversion of the coarse bits is performed with a binary search, such that only 3 comparisons are needed. After the segment is selected, the reference voltage of that segment is reused as a reference to resolve the remaining fine bits. The fine 8-bit conversion is done in the typical SAR algorithm with binary-weighted capacitors.

This architecture addresses the first challenge of the DAC area by reducing the number of capacitors required to achieve high bit resolution. The fine 8 bits set the number of total unit capacitors needed, which in this case are only 256. The second challenge, of capacitor ratio matching, is alleviated by the two-step approach of the A/D conversion. This approach was demonstrated in [5], where the matching requirement to achieve good DNL is set by the number of fine bits. In our case, the matching requirement of the capacitors is 8 bits, which can be easily achieved using good layout practices.

One key advantage of the multi-segment SAR approach, compared with that of the multiple-slope ramping ADC, is that DC reference voltages, and not time-variant slopes, set the segments. DC reference voltage is far easier to control in terms of variation from column to column. As long as the reference voltage settles during each successive approximation decision, there is no issue with reference level variations that might depend on the input signal levels. To address the third challenge of scalability, the reference voltages are routed periodically to external decoupling caps in a block design approach. Figure 4 shows a block diagram of the architecture. With this routing, the settling of the ADC reference voltages no longer depends on the total column size.

The ADC is designed in a 5V/1.8V process, and the ADC reference voltage is set at 4V. The lowest segment starts at 16-bit resolution. Each subsequent segment doubles in LSB size, which, in this design, is set at 62.5 μV. Figure 2 shows a simplified diagram of the A/D conversion process. The companding ADC transfer function and quantization noise-versus-input signal level are shown in Figure 5. A de-companding look-up table is used to linearize the output back to 16-bit levels.

III. Multi-Stage Comparator Design

Figure 3 shows the multi-stage preamp (A_1, A_2 and A_3) and comparator design. In order to minimize the offset of the ADC down to the lowest segment LSB, a high-gain preamp comparator is needed. The gain of the preamp is designed to be large enough to amplify the input signal and overcome the offset of the comparator latch (V_{OSL}), leaving a reduced residual input referred offset ($V_{OSL(res)}$).

$$V_{OSL(res)} = \frac{V_{OSL}}{A_1.A_2.A_3}$$

A three-stage preamp is designed with a combination of both input-offset storage and charge-injection-output storage to minimize the offset. The offsets of the preamps are not amplified, while the charge injection from auto-zero switches is minimized. This prevents the opamp output from saturating while providing high-enough transient open-loop gain to overcome the comparator offset. The charge injection of the auto-zeroing switches is stored sequentially on each output capacitor, after being divided by the gain of its preamp stage. The sequential switching, in addition to bottom-plate input capacitor sampling, minimizes the residual charge injection ($V_{Ch(res)}$) remaining in this capacitive switching network.

$$V_{Ch(res)} = \frac{\Delta q_0 / C_0}{A_1 . A_2 . A_3} + \frac{\Delta q_1 / C_1}{A_2 . A_3} + \frac{\Delta q_2 / C_2}{A_3}$$

IV. Result

A prototype high-speed, column-parallel image sensor was designed with the MS-SAR architecture and fabricated in a 0.18 um 5V/1.8V CMOS process. Analog test inputs were used to inject a known analog input voltage and to characterize the ADC. The measured DNL and INL performance of a typical ADC at the first segment is shown in Figure 6. And finally a sample raw color image taken with the prototype sensor is shown in Figure 7.

V. Acknowledgment

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References

[1] O.-B. Kwon et al., “A novel double slope analog-to-digital converter for a high-quality 640480 CMOS imaging system,” in Proc. IEEE Int. Conf. VLSI and CAD, Oct. 1999, pp. 335–338.
[2] T. Otaka et al., “12-bit column-parallel ADC with accelerated ramp,” in Proc. IEEEWorkshop CCDs Adv. Image Sensors, Karuizawa, Japan, Jun. 2005, pp. 173–176.
[3] Snoeij et al., “Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors,” IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2968-2977, Dec. 2007.
[4] Matsuo et al., “8.9-Megapixel Video Image Sensor with 14-b Column-Parallel SA-ADC,” IEEE Transactions on Electron Devices, vol. 56, no. 11, pp. 2380-2389, Nov. 2009.
[5] Fotouhi and Hodges, “High-Resolution A/D Conversion in MOS/LSI,” IEEE J. Solid-State Circuits, vol. SC-14, no. 6, pp. 920-926, Dec. 1979.

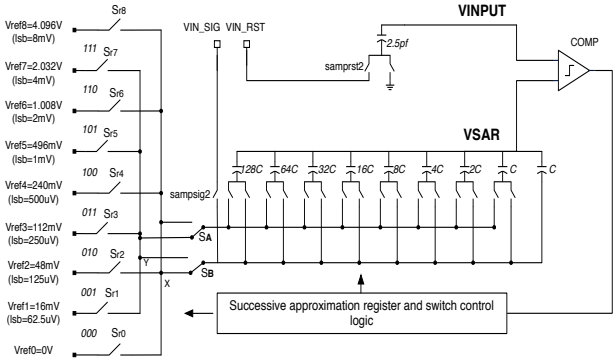


Figure 1. Block Diagram

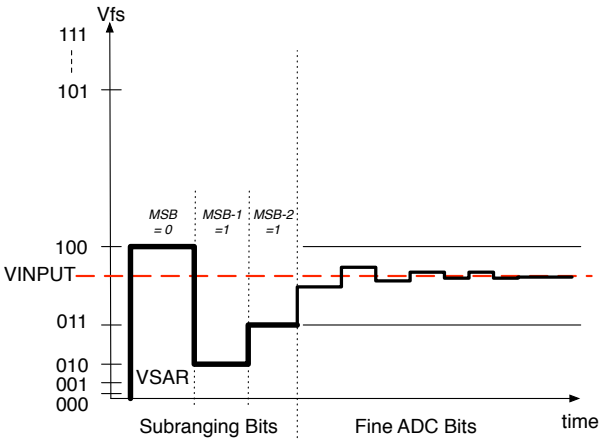


Figure 2. ADC Conversion Process

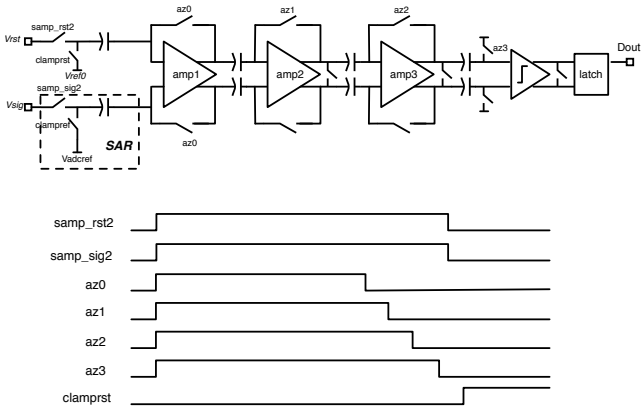


Figure 3. High Gain Comparator

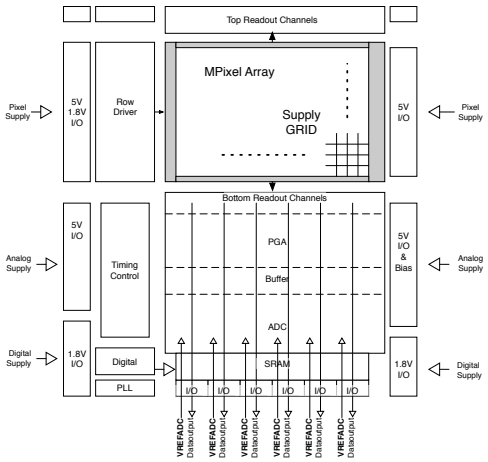
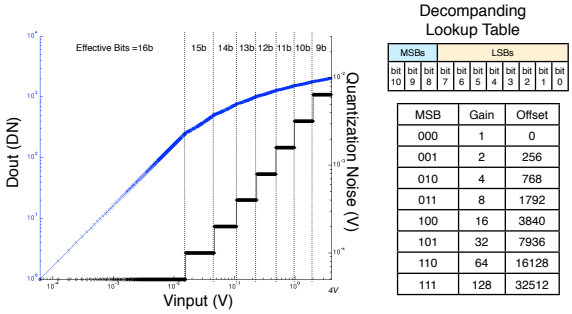


Figure 4. Prototype Sensor



Decompanding Lookup Table

MSBs			LSBs							
bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

MSB	Gain	Offset
000	1	0
001	2	256
010	4	768
011	8	1792
100	16	3840
101	32	7936
110	64	16128
111	128	32512

Figure 5. ADC Transfer Function

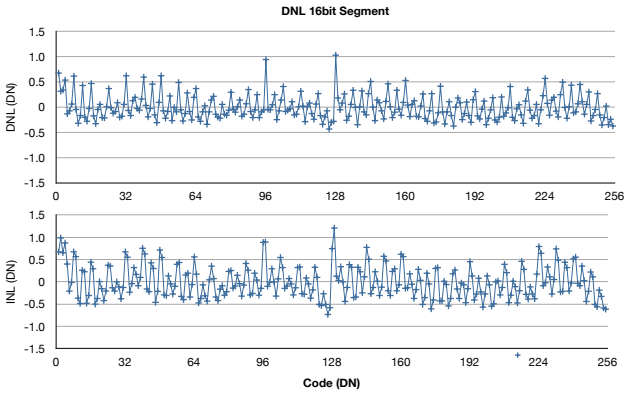


Figure 6. DNL and INL of 16bit Segment

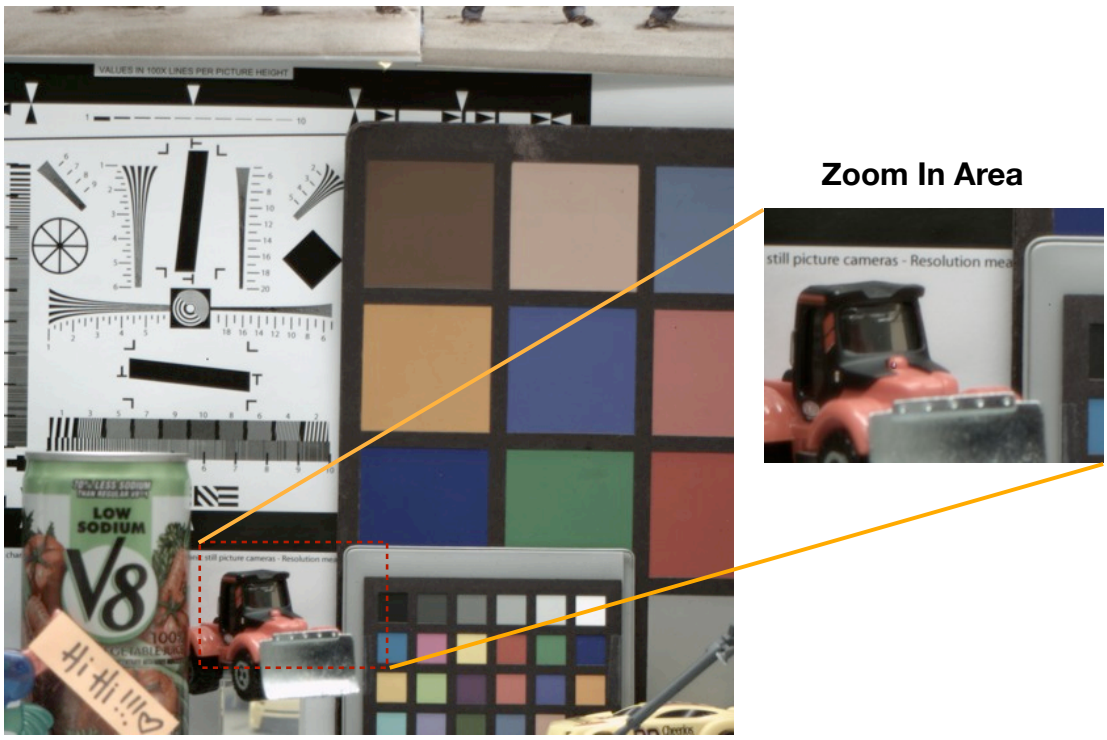


Figure 7. Reproduced Raw Color Image