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RF Design Issues and Challenges in a CMOS Image Sensor Process

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Abstract
This paper presents design issues and challenges encountered when designing RF transceiver circuits in a 0.18 um 3.3V/1.8V CMOS Image Sensor (CIS) process. Even before putting down a transistor to design, there are infrastructure challenges to overcome. These challenges include getting the appropriate models from the foundry, setting up the design environment, generating parasitic extraction decks, and modeling the inductors. After overcoming the huddles of getting the design environment in place, we adopted several general design practices to realize RF transceiver circuits in a CIS process.

I. Introduction

With the rapid development of on-body medical monitoring devices, there is a need to combine the abilities for light sensing and wireless communication on a single die. These medical devices are likely to be disposable and must be produced at reduced cost, low system complexity, low power and small die area. To meet the above requirements, wireless capability needs to be realized in a CIS process. However, some of the optimization in the CIS process for pixel performance conflicts with requirements for typical RF designs. For this reason, some compromises must be made to the process and some new design methods have to be adopted.

II. Infrastructure Challenges

One basic design component in RF transceiver circuits at 2.4GHz is a good inductor with a decent Q factor. However, an inductor is almost never a standard device found in a CIS process. So the first challenge is to convince the foundry to alter its standard CIS flow to include inductors. Since the design environment for the new flow does not exist, we worked closely with the foundry to determine the exact metal stack to generate a specialized PDK with proper LVS, DRC, Density, Antenna, and RCX decks. Many hours of work must be spent verifying and validating the PDK before the design can even begin.

In a typical front side illuminated CIS process, the metal stack normally consists of four layers of thinned down metals sandwiched between thinned down oxides to bring the micro lenses closer to the photodiode to reduce optical crosstalk. But this optimization results in higher metal resistance and higher parasitic capacitance, both of which are not desirable for high-speed designs.

The first alteration is to stay with four layers of metal but use the standard metal thickness option. Utilizing the Berkeley's ASITIC tool to model the inductors in these conditions, we quickly realize these inductors cannot achieve a Q factor of >4 at 2.4GHz due to high coil resistance and high parasitic capacitance to the substrate, rendering them useless in our design. The second alteration is to add a 2 um thick metal five for the inductor. This time, using SONNET's 3D Planar EM Solver, we found that the Q factor is greatly improved. Figure 1 shows

the results of a typical 2D and 3D modeling and simulation using SONNET EM method for the modified CIS metal stack.

III. Design Challenges

Figure 2 shows a typical example of an RF transceiver building block – a differential CMOS LC-VCO. To design a RF PLL, LC-VCO is the only choice because of its advantages in lower phase noise and power consumption. The phase noise performance of a LC-VCO is dominated by the quality factor of the inductors. Therefore much effort and time was spent to change the metal stack and accurately model the inductors to support the PLL design.

In choosing standard metal stack and adding a 2um thick fifth metal, we are optimizing the stack for inductor performance while sacrificing pixel optical cross talk performance. Fortunately in our bio-sensing application, the pixel dimensions are greater than 100um x 100um and the spacing is greater than 10um so we can safely make this tradeoff.

Epitaxy is the standard starting material in a CIS process for its better pixel performances, such as higher QE at longer wavelengths and lower dark current, while bulk is preferred for RF circuits for its higher inductor quality factor. However, our SONNET EM Solver model shows that the epitaxy material does not degrade the quality factor of the inductor until frequencies greater than 5GHz, leading us to choose the epitaxy starting material.

Parasitic capacitances also contribute towards degrading the PLL's phase noise performance and increasing power consumption. After several cycles of layout optimization, extraction, and simulations, we came up with a layout strategy to help reduce parasitic capacitances, which improve phase noise performance and lower power consumption while trading off in a small area increase.

Finally to minimize noise coupling between the RF and sensor circuits, we separate their power and ground rails, time multiplex their on-time, and physically locate the RF circuits as far as possible from the photodiodes.

IV. Results and Conclusion

A test chip was designed with both RF transceiver and sensor circuits and fabricated in the modified five metal 0.18 um 3.3V/1.8V CIS process. Preliminary data from the test chip shows good correlation between measured and simulated performance, validating our PDK modifications and inductor modeling. The simulated and measured PLL tuning curves are shown in Figure 3 and Figure 4 respectively. The simulated tuning curves span a frequency range of 2.25GHz to 2.55 GHz compare to the measured range of 2.28 GHz to 2.55GHz. The simulated and measured PLL phase noise is shown in Figure 5 and Figure 6 respectively. At particular frequencies of interest like 0.1, 1, 10 MHz, the measured phase noise is less than 3dBc/Hz higher than those simulated.

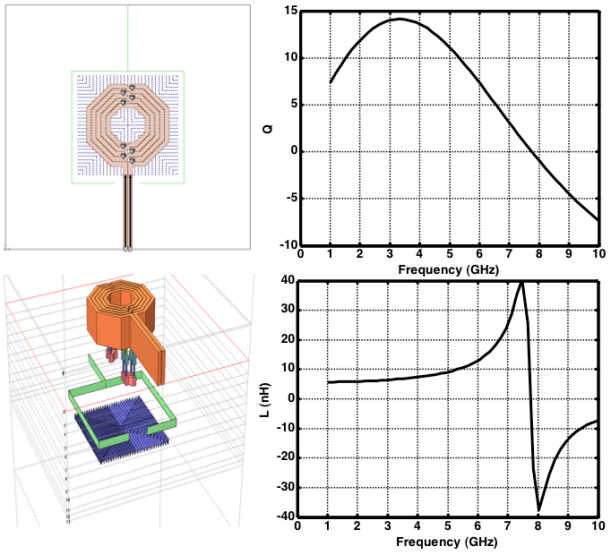

Figure 1 – SONNET 2D, 3D and Inductor Model

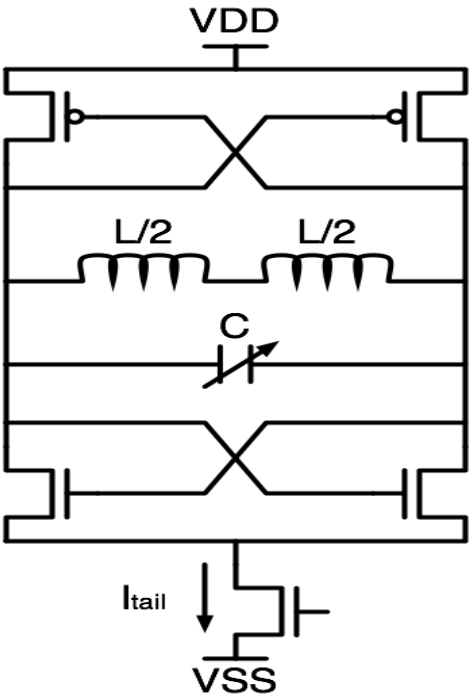

Figure 2 – Typical CMOS LC-VCO Diagram

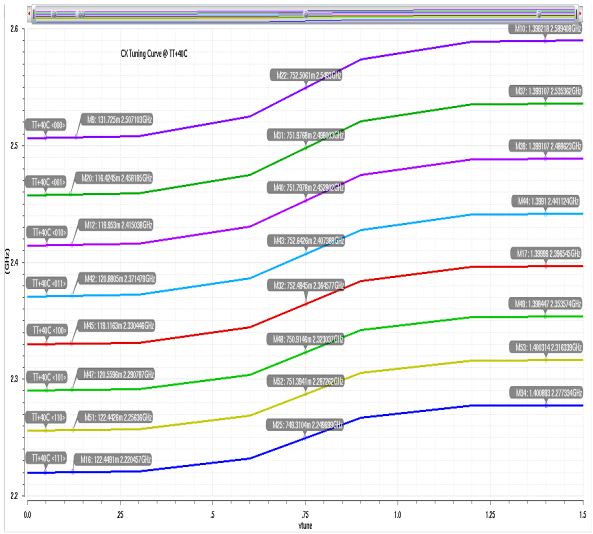

Figure 3 – Simulated PLL Tuning Curves

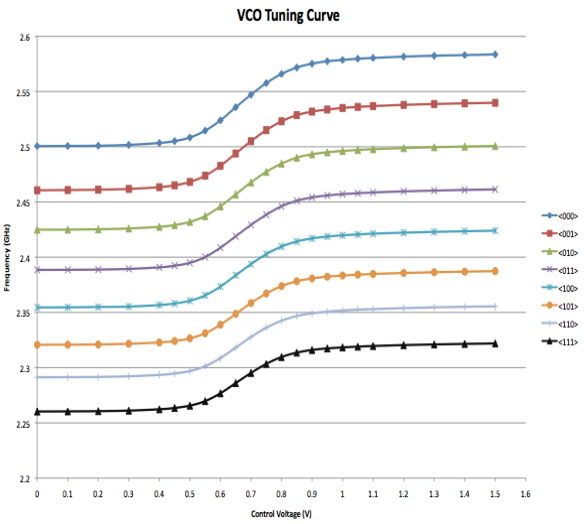

Figure 4 – Measured PLL Tuning Curves

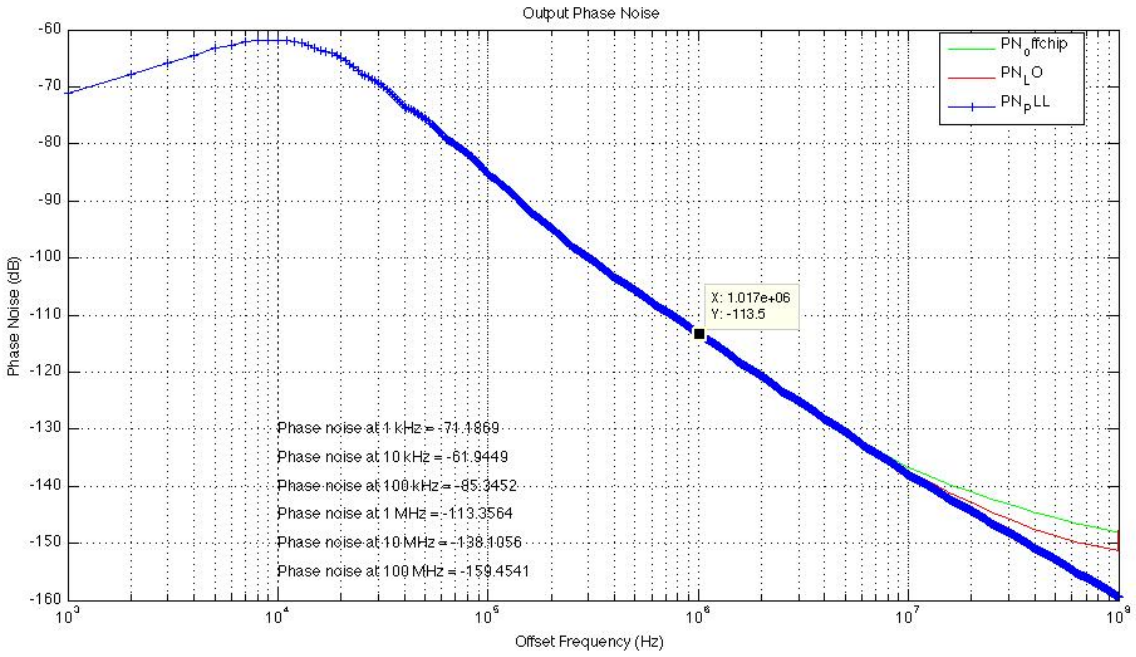

Figure 5 – Simulated PLL Phase Noise

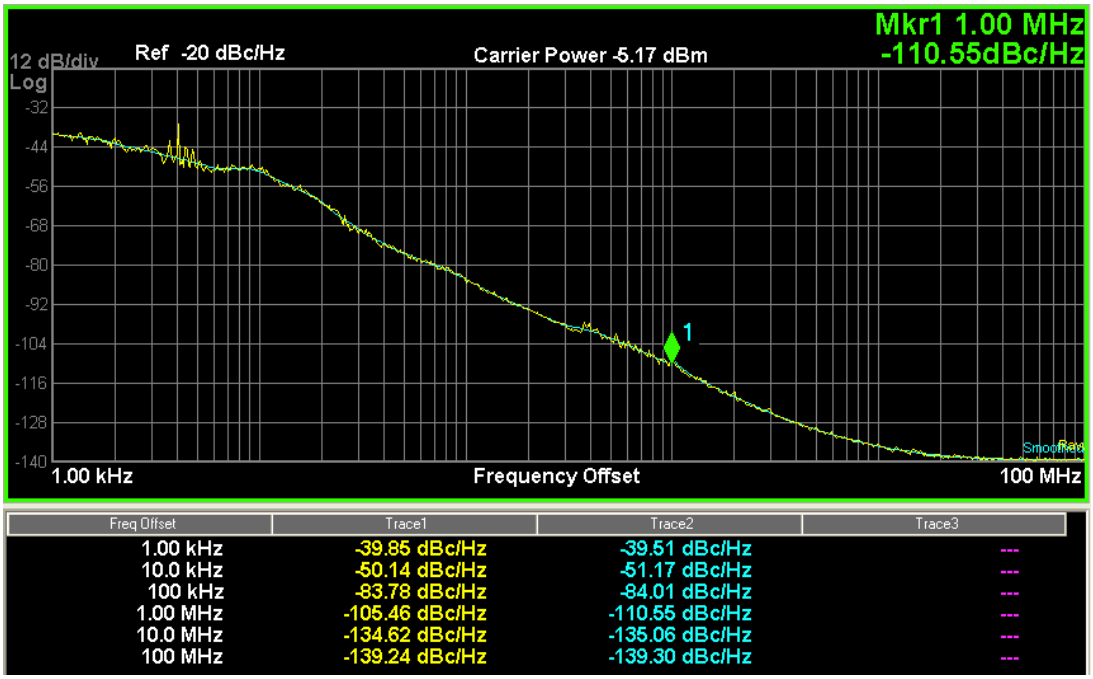

Figure 6 – Measured PLL Phase Noise