Design of Analog Readout Circuitry with Front-end Multiplexing for Column Parallel Image Sensors

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Abstract: This paper reports progress in our design of column parallel analog signal chain with varying degrees of parallelism for CMOS image sensors. In [1] we investigated the trade-offs for different choices of parallelism and presented an analytical model for optimization of an endoscopic sensor. We continue to use the analytical model and have developed an improved analog readout circuitry that enables us to reduced silicon area, achieve higher frame rates, while improving SNR performance. It features a fully differential readout with a high-speed successive approximation A/D converter (SAR-ADC). The analog readout circuitry presented here was designed in a prototype sensor fabricated in 0.18um 3.3V/1.8V CMOS process. The measured results from the prototype sensor shows the signal chain achieving 248uV input referred noise with a throughput of 17.5Mpixel/sec while consuming an estimated 126uW per pixel column.

Figure 1 shows the block diagram of the analog readout circuit. It consists of an array of M sample and hold capacitors followed by the charge mode readout circuit. The charge mode readout stage functions as a level shifter to convert the sample and hold signal to fully differential and as a buffer to drive the signal into the differential SAR-ADC.

Figure 2 shows the result of our analytical model, which we used to optimize the number of columns to multiplex into the readout circuit. In this case, M=32 was selected in order to trade-off noise for lower area and power consumption.

Figure 3 shows the schematic of the charge mode readout amplifier. The amplifier topology chosen was a two-stage amplifier with a folded cascode first stage followed by a common source second stage. The second stage topology was chosen to achieve maximum output swing for a given supply voltage.

Figure 4 shows a simplified block diagram of the SAR-ADC. The ADC adopts a sub-radix 2 architecture, which allows for incomplete reference voltage settling and therefore increased conversion rate. It also features additional capacitors for reference error adjustment and foreground calibration of the non-binary weighted SAR. The ADC outputs 14-bits sub-radix2 that then gets converted to binary 12-bits.

References:

[1] D. Van Blerkom, et al., "Analysis of Front-end Multiplexing for Column Parallel Image Sensors," in *2011 International Image Sensor Workshop,* Hokkaido, Japan, June 2011.
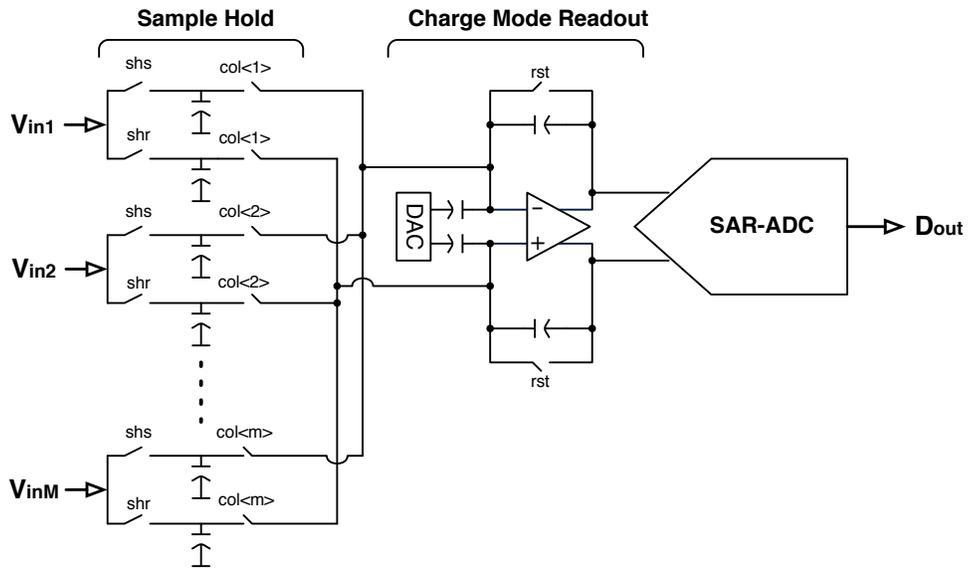
Figure 1. Analog Readout Circuitry Block Diagram
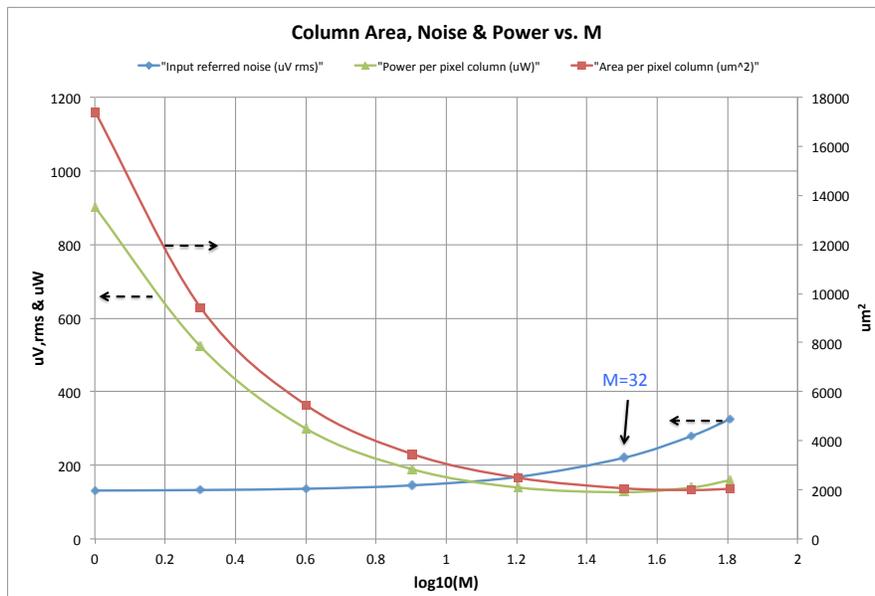
Figure 2. Analytical Model for Trade-off
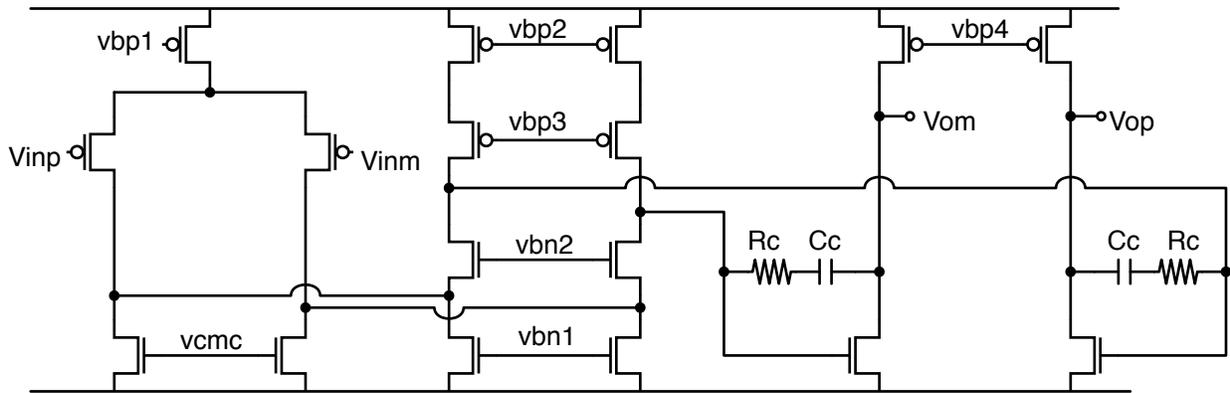
Figure3. Charge Mode Readout Amplifier
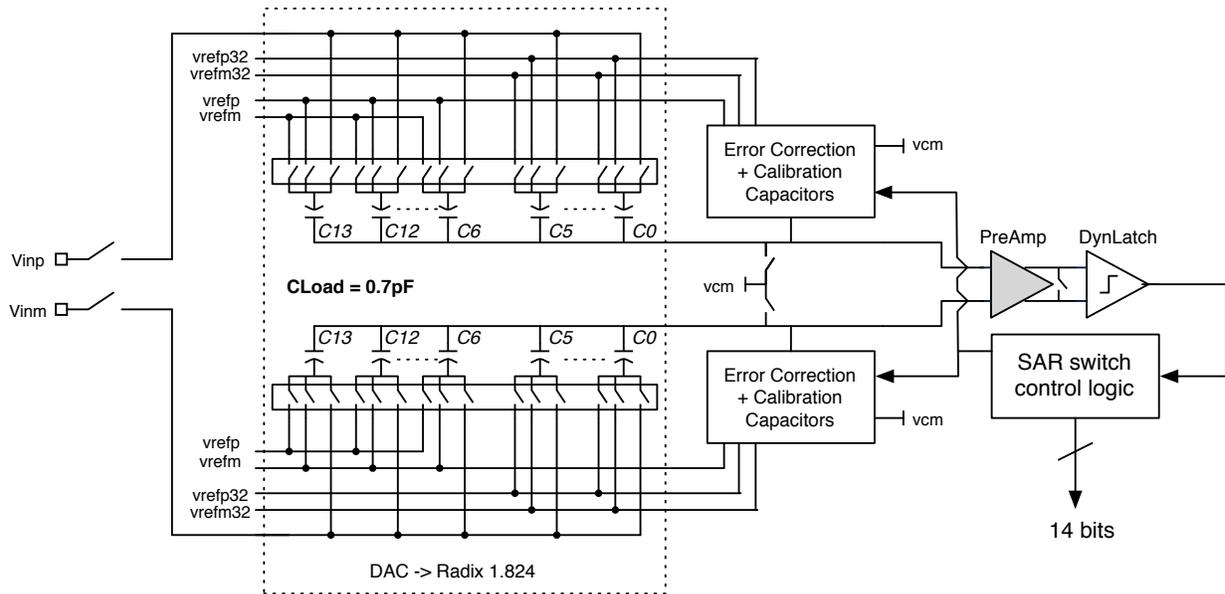
Figure 4. Sub-Radix2 SAR-ADC