CMOS Sum & Difference Imager with On-Chip Charge-Leakage Compensation

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Abstract

This paper presents a new technique for implementing a low-power CMOS imager with simultaneous on-chip computation of the difference and sum of two successive frames. Existing difference imagers are susceptible to errors due to collection (by the sense element and in-pixel storage node) of photo-generated charge that diffuses from the photo-active pixel area during integration of the second frame. Our proof-of-concept imager uses a new unbalanced differential signal chain to provide 17 fold reduction in leakage error in the frame-difference output. The resulting INL is < 1 % over most of the illumination range. Error reduction is achieved without noticeable increase either of fixed-pattern-noise (FPN) or of read noise, preserving high image quality. Power dissipation in the 256x256 imager is measured to be only 18 mW.

1. Introduction

CMOS imagers have made rapid progress in recent years for multi-media applications such as motion detection, motion-estimation, video compression, object segmentation through boundary detection, and surveillance systems. These applications often require computation of difference between the outputs of successive frames. On-chip computation of the frame-difference increases the effective data rate while eliminating the need for external frame memory, enabling system power savings and miniaturization. A frame-difference imager simultaneously allows high computation accuracy and high update rates. This is especially true for cases where small differences between two large signals are measured, in which case on-chip difference computation allows the imager output to be digitized using lower resolution analog-to-digital converters (ADC), enabling the use of high-speed converters.

On-focal-plane frame difference computational imagers have been reported earlier using both photogate [1] and photodiode approaches [2]. In either case, the pixel features an in-pixel storage element that holds the signal from the previous frame, while the current frame is being exposed. Since a CMOS imager typically uses a differential signal chain, frame-difference is computed on a pixel-by-pixel basis by subtracting the current frame value from the stored frame value in the imager signal chain.

The main problem in either approach is the corruption of the stored frame during the current frame exposure by the collection (at the optically shielded sense and storage elements) of photo-generated electrons that diffuse from the photo-active pixel area. Such leakage errors are necessarily pixel implementation dependent, but can easily be very large for an imager implemented in sub-micron CMOS technology, vastly degrading image contrast and introducing inaccuracies. Most importantly, since the signal mixing occurs at the pixel level, no post-processing techniques can correct for the errors once an on-chip difference computation has been carried out. Similarly, extra transistor switches and/or the use of double-poly storage capacitors may reduce the leakage, but only with an unacceptable loss in fill factor or unacceptable increase in pixel size. Even then, further leakage compensation may be necessary, especially for scientific applications. These issues have not been systematically addressed in previous reports.

2. Theory of operation

Figures 1 illustrates the pixel schematic of the CMOS difference imager reported in this paper. The pixel consists of a photogate (PG) under which photoelectrons are accumulated during exposure, a transfer gate (TX) for transferring the

electrons from PG to the sense node (SENSE), implemented as a reverse-biased p-n junction. The sense node also acts as an in-pixel frame memory. It is covered by metal to provide optical shielding. For resetting and reading out the pixel, the source-follower (M_{sf}), selection (M_{sel}), and reset (M_{rst}) FETs are used. In addition to the floating diffusion, the sense node consists of a FET connected as a capacitor (Cs) to increase the sense node capacitance for operation in high-flux conditions, requiring a large full-well capacity.

Under normal imaging mode, the sense node is sampled twice: once after it is reset by momentarily pulsing M_{rst} high, and a second time, after the photoelectrons are transferred into the sense node by momentarily pulsing PG low. By computing the difference between the samples, the imager provides a signal proportional to the photoelectrons collected in each pixel. Differential readout also ensures FPN suppression via elimination of offsets due to pixel-to-pixel threshold mismatches.

For frame-difference mode operation, the sense node is used for storing the previous frame signal. During readout, the previous frame signal stored on the sense node is sampled first, followed by a reset, and sampling of the current frame signal that was accumulated under PG. Sample-and-hold capacitors at the bottom of the column store the signals from the two successive frames. Since the signal chain is differential, the frame-difference is automatically computed. An unbalanced (i.e. variable gains on the two branches) differential signal chain provides for the leakage error correction. The chip output is thus given by:

$$V_{out} = V_1 - g_2 \cdot V_2 = g \cdot (N_1 - N_2 \cdot \{g_2 - \delta\})$$

where V_1 and V_2 are the frame 1 & frame 2 signals, respectively, g and g_2 are the overall amplifier gain and δ is the gain correction necessary to eliminate the leakage error. By choosing $g_2 = 1 + \delta$, the leakage error can be made arbitrarily small. The gain stages are implemented using a fully-differential switched-capacitor signal chain, that consists of two global opamps with variable feedback capacitors to provide the necessary difference in gain between the two branches.

In conventional imagers, pixel-to-pixel offset correction and flicker noise suppression depend upon exact difference computation, (i.e. equal gain on both sides of the differential chain). In order to ensure that the difference in gains does not cause increased FPN, the gain stages are preceded offset correction stages. The column-based offset cancellation circuit generates charge packets proportional to the difference of the two pixel samples. As a result, the source follower threshold voltage appears in the common mode, and hence any pixel-to-pixel threshold variation is rejected by the differential signal chain that follows it. By amplifying the offset-corrected charge, both leakage-error and FPN correction occurs simultaneously. The read noise of the device is limited by the front end – i.e. the pixel reset noise. Since the signal chain noise is smaller compared to the pixel noise, and since the gain variation in the signal chain is ~ 15-20% at the most, the read noise does not increase due to unbalancing of the signal chain.

The frame sum is generated using a similar differential signal chain to the difference circuit, but with a different timing sequence. It should be emphasized that leakage compensation also enables the original frame images to be determined from just the sum and difference images, if necessary. Only the frame difference output is discussed in this paper, since the leakage compensation technique is the crucial element for both sum and difference outputs.

3. Results

Figure 2 illustrates the layout of the 256x256 proof-of-concept imager which was implemented in a 0.5 μm single poly, triple metal CMOS technology made available through MOSIS. The photogate imager was implemented in a 15x15 μm pixel pitch. The total chip area is 5.6 mm x 5.8 mm, of which the imager area is 3.85 mm x 3.85 mm.

“White” light tests were carried out using a grey-scale bar-pattern target with > 180x reflectivity variation. Images were captured at several different incident lamp intensities to cover the imager dynamic range. Figure 3a shows the direct mode image of the target pattern at a mean signal of 260 mV, figure 3b is captured in difference mode under the same illumination and without any error correction. Figure 3c is captured in the difference mode with the previously described, single point, gain adjustment. Ideally, the images in figure 3b and 3c should be uniformly grey. However, a

significant amount of residual pattern can be seen in figure 3b, due to charge leakage from the current frame into the storage nodes. The image in figure 3b indicates that without error correction, frame-difference imaging is not very practical. Figure 3c shows that once the error correction is applied, the residual pattern is practically invisible, except in regions of the largest intensity changes. The appearance of the residual pattern is due to pixel-to-pixel cross-talk, and can be minimized through appropriate layout that moves the storage node away from the pixel edges.

Figure 4 shows data on the leakage-compensated frame-difference imager output as a function of the actual difference of the frame 1 and frame 2 signals. Excellent charge leakage error suppression is indicated by the linear difference output over a 100x range of intensity differences in either of the two frames. After correction, the residual error is both small (< 1.5%) and constant across the entire signal range, indicating a 17x reduction in error. A red LED was used in these measurements as a worst-case test because the longer wavelength is absorbed deeper in the silicon substrate, leading to higher leakage errors via diffusion-induced charge collection. The <1% Integral Non-Linearity (INL) in Figure 5 indicates the significant reduction of charge leakage error over the entire illumination range.

Dark, flat field images showed no noticeable column FPN. Changing the gain of the two branches has no discernible effect on the read noise which remains fixed at 250 μV, and is entirely accounted for by pixel reset noise. Imager performance is summarized in table 1.

4. Conclusions

A new technique for on-chip frame-difference imaging circuit is presented. The imager provides both direct and difference mode output, with errors due to charge leakage from one frame to another via substrate diffusion suppressed to invisible levels. Error compensation is achieved by providing different gains in the two branches of the differential signal chain. A single point gain adjustment is capable of yielding INL < 1% over a very large range of illumination. The error correction does not affect the imager FPN or random noise. The 18 mW power dissipation, makes it greatly attractive for portable applications.

5. Acknowledgement

The work described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

6. References

[1] S. Ma and L. Chen, "A single chip CMOS APS camera with direct frame difference output", *IEEE J. of Solid-State Circuits*, Vol. SC-34, p 1415-1418, 1999.

[2] A. Dickinson, et al., "A 256x256 CMOS active pixel image sensor with motion detection", *Tech. Dig. IEEE ISSCC*, Vol. 38, p 226-227, 1995.

Table 1. Performance Characteristics

Characteristics	Values	Comments
Format	256x256	
Pixel	15 μm x 15 μm	Photo-gate
CMOS tech.	0.5 μm 1P3M	
Responsivity	1.9 μV/e^-	Broad-band ill.
Full-well	500,000 e^-	
Uncorrected error	25%	@ 650 nm
Corrected residue	< 1.5%	> 17x reduction
INL	<1 %	over 95 % of range
Read Noise	250 μV	Std. Dev.
FPN	150 μV	Std. Dev.
Power dissipation	18 mW	@ 3.3V

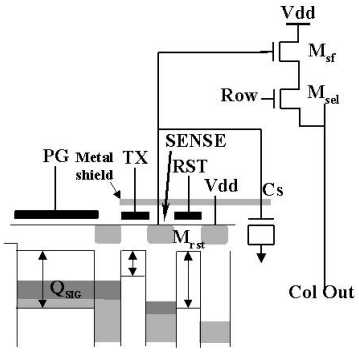


Figure 1. Schematic diagram of the frame-difference imager pixel circuit. The sense node, covered by metal for optical shielding, provides in-pixel frame memory. The FET capacitor (Cs) enables high-flux operation.

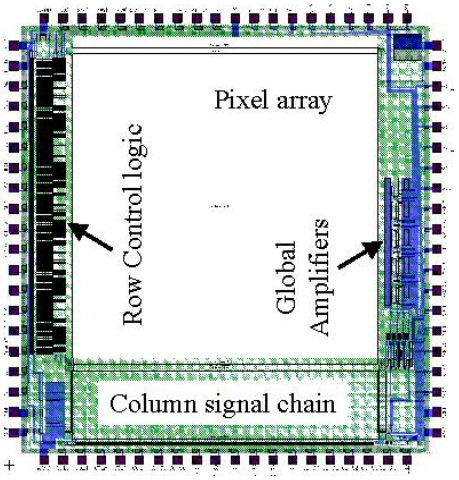
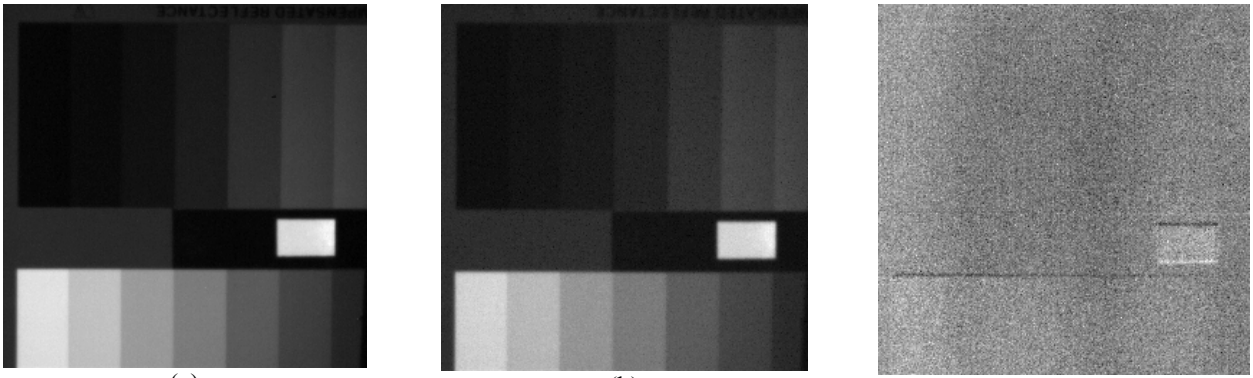


Figure 2. Imager layout with component blocks.



(a) (b) (c)

Figure 3. **(a)** Direct mode image of gray scale bar-pattern with >180x reflectivity variation, under "white light" illumination. **(b)** Difference mode image without error correction. **(c)** Difference mode image after error correction.

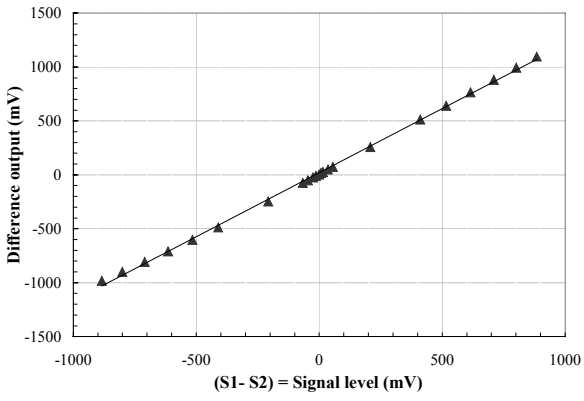


Figure 5. Frame-difference output as a function of the actual intensities in the two frames under flat-field, red LED illumination.

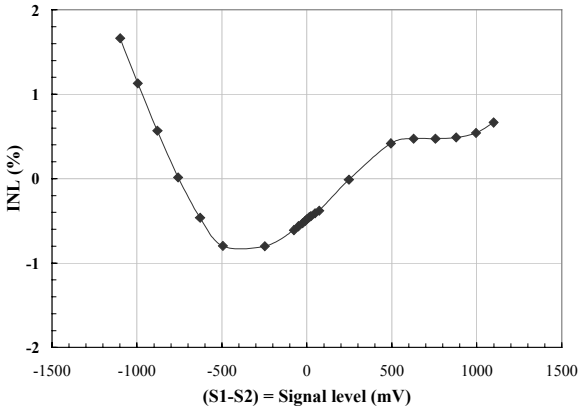


Figure 6. Integral Non-Linearity (INL) of the difference output after leakage correction, under flat-field, red LED illumination.